In all the examples of gridistors that have been given above, the drain region is formed in the substrate and the source region in the epitaxial layer. To reduce the source-grid capacitance in this case, it is of advantage to select a higher resistivity for the epitaxial layer **3** than for the substrate **1**. For example, for the substrate a resistivity 2 ohms-cms. can be taken and for the epitaxial layer a resistivity of 4 to 6 ohm-cms.

Two consequences result from this. Firstly, the grid-source capacitance is significantly reduced since it is almost inversely proportional to the square root of the resistivity. Secondly, the saturation characteristic of the current is improved and FIG. 14 explains this apparently surprising consequence. In actual fact, although it is quite exact that this hardly changes the diffusion profile of the grid, on the other hand the profile of the channels is quite considerably modified due to the depletion space developed at the p-n junction between the grid and the channel. This is shown by the curves in FIG. 14, in a particular case characterized by the following parameters:

Resistivity of the substrate: 1 ohm-cm.
Resistivity of the epitaxial layer: 2.5 ohm-cms.
Theoretical diameter of the channel: 2μ
Thickness of the grid: 3μ

In FIG. 14, the two half-circles in thin lines **55** show the thoretical profile of the channel in a plane passing through its axis when the depletion layer is cancelled out by opposite biasing of the grid compensating the potential barrier of the junction; this is a circular profile. The heavy line curve **57** shows the profile in the absence of any biasing, account being taken of the natural depletion spaces of the p-n junction in the case of the epitaxial layer resistivity being higher than the substrate resistivity. Finally, broken line **56**, for the portion of the channel located in the epitaxial layer, corresponds to the case where resistivity of this layer would be equal to that of the substrate. This makes it possible to appreciate the improvement obtained. It can thus be seen that, whereas in the latter case (same resistivities on both sides of the line separating the epitaxial layer and the substrate), the profile of the channel is rapidly flared on both sides, thereby impeding the drain current saturation process, in the case according to the invention (curve **57**), the profile becomes much more similar to a truncated cone with a relatively small angle at the tip, the advantages of which are disclosed in U.S. Patent No. 2,939,057 issued May 31, 1960 to the present applicant.

It can however be interesting, as will be shown, to simultaneously invert the locations of the source and drain electrodes, as well as the resistivity values of the layers (epitaxial layer and substrate) adjacent to these two electrodes. This will be shown in relation to FIGS. 15 and 16.

FIG. 15 shows the typical profile of an elementary channel **37** running from source **39** to drain **36** and surrounded by a grid mesh **34**. The depletion space **89** delimiting the profile of the channel is developed by the field-effect produced by the voltage applied between source **39** and drain **36** and then between grid mesh **34** and drain **36**, the grid being assumed to be directly connected to the source.

Such a structure can be represented, essentially, by the equivalent diagram in FIG. 16 where:

Resistors 91_1, 91_2, 91_3, 91_4, 91_5, 91_6 are resistors distributed along the entire length of channel **37**, with values increasing from the source extremity to the drain extremity as a result of throttling in the channel section, this increase of the resistance per unit length being further and considerably accentuated by the reduction in the mobility of the charge carriers as a function of the electrical field strength in the portions of the channel where the field strength exceeds the so-called critical value; -capacitors 92_1, 92_2, 92_3, 92_4, 92_5, 92_6 are distributed capacitors due to the depletion layer **89** between grid mesh **34** and channel **37** with, on the contrary, values decreasing from the source extremity to the drain extremity:

Resistors in series 93_1, 93_2, 93_3, 93_4, 93_5, 93_6 represent the distributed resistance of the grid body between the grid contact through which the grid is biased and the portion of the channel under consideration. These resistors represent the resistances of grid sections from the source extremity to the drain extremity as shown in FIG. 15.

The signal source applied between the source **39** and the grid contact **94**, upstream the grid body resistance, is designated by **95**.

By examining the diagram in FIG. 16, it will be noticed that, to reduce the effect of the time constant on the signal applied between grid and source, with given resistors **91** and capacitors **92**, an attempt must be made, certainly not exclusively, but particularly to reduce the parasitic resistances 93_1, 93_2 . . . on the flared part of the channel, since they are associated with capacitors 92_1, 92_2 . . . which are of relatively high capacity value and resistors 91_1, 91_2 . . . which are of relatively low resistance value.

Now, in the present state of manufacturing techniques for gridistor structures, the grid is first diffused into substrate **1**, with continuous supply from an external source of the diffusing element; then the impurities thus accumulated are redistributed by heat treatment, without any further supply of the diffusing element, both in layer **3** and substrate **1**. The volume of impurities previously accumulated in substrate **1** then plays the part of an internal source of diffusing element and it can easily be understood that the resistance of the grid embedded in the substate is necessary less than that of the part of the grid diffused into layer **3**.

It is possible to deduce, from this, the advantage that can be obtained from locating the source region in substrate **1** and, correlatively, the drain region in layer **3**, particularly in the case of structures with fairly large areas in high-frequency gridistores, and, this being, to make the resistivity of substrate **1** at least equal to, and preferably higher than that of layer **3**.

It must be well understood that the above-described shapes, materials and manufacturing processes used to explain the invention, as well as the proposed methods of using the resulting products, have been selected by way of example and could be modified to a large extent without exceeding the scope of the invention.

What I claim is:

1. A multichannel field-effect semiconductor device comprising a substrate wafer of semiconductor material of a given type of conductivity, having source and drain regions on its parallel major faces, a diffused internal grid of the opposite type to said given type of conductivity and bounding a number of conductive channels, said grid including a perforated region defining conductive channels transverse thereto, a solid region and strip regions both devoid of conductive channels, said strip regions extending from said solid region, and a diffused superficial grid contact region of said opposite type of conductivity, disposed above said internal solid and strip regions and in ohmic contact therewith, said strip regions causing said perforated region of said grid to be substantially equipotential.

2. A multichannel field-effect semiconductor device as set forth in claim **1** in which said internal grid solid region and said superficial grid contact region disposed thereabove have the shape of a peripheral frame separating said source and drain regions, and in which said internal gate strip regions and said superficial grid contact region are on the internal side of said frame.

3. A multichannel field-effect semiconductor device as set forth in claim **1** in which said internal grid solid region